11-08-05

Docket No. 8201/Y01/SYNX/JW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re: Inventor(s): Michael R. Rice, Eric A. Englhardt, Vinay Shah, Martin R. Elliott, Robert B. Lowrance and Jeffrey C. Hudgens
Title: SYSTEMS AND METHODS FOR TRANSFERRING SMALL LOT SIZE SUBSTRATE CARRIERS BETWEEN PROCESSING TOOLS
Serial No.: 10/764,620
Filed: January 26, 2004
Examiner: Kasenge, Charles R
Group Art Unit: 2125

Transmitted herewith is:

X PTO Form 1449;

X Information Disclosure Statement, and sixty-seven cited references (copy of fifty-nine references enclosed); and

X Return Postcard.

FEE CALCULATION

Fee Items	Claims Filed	Included With Basic Fee	Extra Claims	Fee Rate	Total
Total Claims	N/A	- 20 =	-0-	X $50.00	$0.00
Independent Claims	N/A	- 3 =	-0-	X $200.00	$0.00
Basic Filing Fee				$790.00	$0.00
TOTAL FEES					PAID

___ The Commissioner is hereby authorized to charge $0.00 to Deposit Account No. 04-1696.

XX The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **04-1696**. A duplicate copy of this transmittal is enclosed.

XX Please address all future correspondence to:

Customer # 41161
Dugan & Dugan, PC
55 South Broadway
Tarrytown, NY 10591

I hereby certify that this correspondence is being deposited with the United States Postal Service as express mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Express Mail Receipt No. EV605115695US

Date of Deposit: November 7, 2005

Signature:

Respectfully submitted,

Brian M. Dugan
Registration No. 41,720
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Express Mail Label No. EV605115695US

PATENTS
8201/Y01/SYNX/JW

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INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97, applicants wish to call the attention of the Examiner to the following references:

U.S. Patent No. 5,544,350, Hung et al.

U.S. Patent No. 5,612,886, Yi-Cherng Weng

U.S. Patent No. 5,818,716, Chin et al.

U.S. Patent No. 5,825,650, Tza-Huei Wang

U.S. Patent No. 5,971,585, Dangat et al.

U.S. Patent No. 6,128,588, Guillermo Rudolfo Chacon

U.S. Patent No. 6,196,001, Tannous et al.

U.S. Patent No. 6,415,260, Yang et al.

Foreign Art Reference No. JP 55091839 A (Japan)

Foreign Art Reference No. JP 58028860 A (Japan)

Foreign Art Reference No. JP 60049623 A (Japan)

Foreign Art Reference No. JP 01181156 A (Japan)

Foreign Art Reference No. JP 01257549 A (Japan)

Foreign Art Reference No. JP 02015647 A (Japan)

Foreign Art Reference No. JP 05128131 A (Japan)

Foreign Art Reference No. JP 05290053 A (Japan)

Foreign Art Reference No. JP 06260545 A (Japan)

Foreign Art Reference No. JP 08249044 A (Japan)

Foreign Art Reference No. JP 09115817 A (Japan)

Foreign Art Reference No. JP 10135096 A (Japan)

Foreign Art Reference No. JP 11176717 A (Japan)

Foreign Art Reference No. JP 11296208 A (Japan)

Foreign Art Reference No. JP 01332464 A (Japan)

Foreign Art Reference No. JP 03007584 A (Japan)

Foreign Art Reference No. DE 19715974 A1 (Germany)

Foreign Art Reference No. EP 1128246 A2 (EPO)

Przewlocki, H. et al., "DIASTEMOS-computerized system of IC manufacturing control and diagnostics", 1990, Elektronika, Vol. 31 No. 11-12, Pgs. 38-40, Polish Language. (Abstract only)

Lovell, A. M. et al., "Cell automation: integrating manufacturing with robotics", Dec. 1990, Solid State Technology, Vol. 33 No. 12, Pg. 37-9.

Prasad, K., "A generic computer simulation model to characterize photolithography manufacturing area in an IC FAB facility", Sept. 1991, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 14 No. 3, Pg. 483-7.

Ehteshami, B. et al., "Trade-offs in cycle time management: hot lots", May 1992, IEEE Transactions on Semiconductor Manufacturing, Vol. 5 No. 2, Pg. 101-6.

Lou, S. et al., "Using simulation to test the robustness of various existing production control policies", 1991, 1991 Winter Simulation Conference Proceedings, IEEE, Pg. 261-9.

Berg, R. et al., " The formula: world class manufacturing for hybrid thin-film component production", 1992, IEEE/SEMI International Semiconductor Manufacturing Science Symposium, Pgs. 53-60.

Naguib, H., "The implementation of total quality management in a semiconductor manufacturing operation", 1992,

IEEE/SEMI International Semiconductor Manufacturing Science Symposium, Pg. 63-7.

Rose, D., "Productivity enhancement", 1992, IEEE/SEMI International Semiconductor Manufacturing Science Symposium, Pg. 68.

Narayanan, S. et al., "Object-oriented simulation to support operator decision making in semiconductor manufacturing", 1992, 1992 IEEE International Conference on Systems, Man and Cybernetics, Vol. 2, Pg 1510-15.

Leonovich, G. A. et al., "Integrated cost and productivity learning in CMOS semiconductor manufacturing", Jan.-March 1995, IBM Journal of Research and Development, Vol. 39 No. 1-2, Pg. 201-13.

Leonovich, G., "An approach for optimizing WIP/cycle time/output in a semiconductor fabricator", 1994, Sixteenth IEEE/CPMT International Electronics Manufacturing Technology Symposium. 'Low-Cost Manufacturing Technologies for Tomorrow's Global Economy'. Proceedings 1994 IEMT Symposium, Vol. 1, Pg. 108-11.

Schomig, A. K. et al., "Performance modelling of pull manufacturing systems with batch servers", 1995, Proceedings 1995 INRIA/IEEE Symposium on Emerging Technologies and Factory Automation. ETFA`95, Vol. 3, Pg. 175-83.

Juba, R. C. et al., "Production improvements using a forward scheduler", 1996, Seventeenth IEEE/CPMT International Electronics Manufacturing Technology Symposium `Manufacturing Technologies - Present and Future`, Pg. 205-9.

Fuller, L. F. et al., "Improving manufacturing performance at the Rochester Institute of Technology integrated circuit factory", 1995, IEEE/SEMI 1995 Advanced Semiconductor Manufacturing Conference and Workshop. Theme - Semiconductor Manufacturing: Economic Solutions for the 21st Century. ASMC `95 Proceedings, Pg. 350-5.

Houmin, Yan et al., "Testing the robustness of two-boundary control policies in semiconductor manufacturing", May 1996, IEEE Transactions on Semiconductor Manufacturing, Vol. 9 No. 2, Pg. 285-8.

Lopez, M. J. et al., "Performance models of systems of multiple cluster tools", 1996, Nineteenth IEEE/CPMT International Electronics Manufacturing Technology Symposium. Proceedings 1996 IEMT Symposium, Pgs. 57-65.

Collins, D. W. et al., "Implementation of Minimum Inventory Variability Scheduling 1-Step Ahead Policy(R) in a large semiconductor manufacturing facility", 1997, 1997 IEEE 6th International Conference on Emerging Technologies and Factory Automation Proceedings, Pgs. 497-504.

Labanowski, L., "Improving overall fabricator performance using the continuous improvement methodology", 1997, 1997 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop. Theme - The Quest for Semiconductor Manufacturing Excellence: Leading the Charge into the 21st Century. ASMC Proceedings, Pg. 405-9.

Dudde, R. et al., "Flexible data registration and automation in semiconductor production", 1997, Proceedings of the SPIE - The International Society for Optical Engineering, Pg. 171-81.

Padillo, J. M. et al., "A strategic domain: IE in the semiconductor industry", March 1998, IIE Solutions, Pgs. 36-40, 42.

Collins, D. W. et al., "Investigation of minimum inventory variability scheduling policies in a large semiconductor manufacturing facility", 1997, Proceedings of the 1997 American Control Conference, Vol. 3, Pg. 1924-8.

Rose, O., " WIP evolution of a semiconductor factory after a bottleneck workcenter breakdown", 1998, 1998 Winter Simulation Conference. Proceedings, Vol. 2, Pgs. 997-1003.

Iriuchijima, K. et al., "WIP allocation planning for semiconductor factories", 1998, Proceedings of the 37th IEEE Conference on Decision and Control, Vol. 3, Pg. 2716-21.

Weiss, M., "New twists on 300 mm fab design and layout", July 1999, Semiconductor International, Vol. 22 No. 8, Pgs. 103-4, 106, 108.

Van Antwerp, K. et al., "Improving work-in-progress visibility with active product tags ÝASIC manufacture", Oct. 1999, Micro, Vol. 17 No. 9, Pgs. 67-9, 72-3.

Martin, D. P., " Total operational efficiency (TOE): the determination of two capacity and cycle time components and their relationship to productivity improvements in a semiconductor manufacturing line", 1999, 10th Annual IEEE/SEMI. Advanced Semiconductor Manufacturing Conference and Workshop. ASMC 99 Proceedings, Pgs. 37-41.

Martin, D. P., "Capacity and cycle time-throughput understanding system (CAC-TUS) an analysis tool to determine the components of capacity and cycle time in a semiconductor manufacturing line", 1999, 10th Annual IEEE/SEMI. Advanced Semiconductor Manufacturing Conference and Workshop. ASMC 99 Proceedings, Pg. 127-31.

Marcoux, P. et al., "Determining capacity loss from operational and technical deployment practices in a semiconductor manufacturing line", 1999, 1999 IEEE International Symposium on Semiconductor Manufacturing Conference Proceedings, Pg. 3-5.

Chen, J. C. et al., "Capacity planning for a twin fab", 1999, 1999 IEEE International Symposium on Semiconductor Manufacturing Conference Proceedings, Pg. 317-20.

Wei Jun-Hu et al., "Optimization methodology in simulation-based scheduling for semiconductor manufacturing", Oct. 2000, Information and Control, Vol. 29 No. 5, Pg. 425-30, Chinese language. (Abstract only)

Hughlett, E., "Incremental levels of automation in the compound semiconductor fab", Aug. 2001, Compound Semiconductor, Vol. 7 No. 7, Pg. 69-73.

Sarin, S. C. et al., "Reduction of average cycle time at a wafer fabrication facility", 2001, 2001 GaAs MANTECH Conference. Digest of Papers, Pg. 241-6.

Saito, K. et al., "A simulation study on periodical priority dispatching of WIP for product-mix fabrication", 2002, 13th Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference. Advancing the Science and Technology of Semiconductor Manufacturing. ASMC 2002, Pg. 33-7.

Wang, J. et al., "The improvement of automated material handling system traffic control", 2002, 2002 Semiconductor Manufacturing Technology Workshop, Pg. 271-4.

Wei Jie Lee, "Optimize WIP scale through simulation approach with WIP, turn-over rate and cycle time regression

analysis in semiconductor fabrication", 2002, 2002 Semiconductor Manufacturing Technology Workshop, Pg. 299-301.

Young Hoon Lee et al., "Push-pull production planning of the re-entrant process", 2003, International Journal of Advanced Manufacturing Technology, Vol. 22 No. 11-12, Pg. 922-31.

Garlid, Scott C., "From philosophy to reality. Interpreting the rules of JIT for IC manufacturing", 1989, SME Technical Paper (Series) MS. Publ by SME, Pg. 797.

Anon, " Wafer level automation", Jan. 1995, European Semiconductor, Vol. 17 No. 1, Pg. 2.

Anon, "Coming of fab-wide automation", May 1998, European Semiconductor Design Production Assembly, Vol. 20 No. 5, Pg. 21-22.

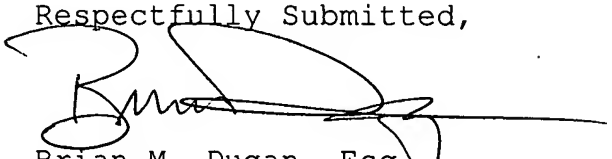
Pierce, Neal G. et al., "Dynamic dispatch and graphical monitoring system", 1999, IEEE International Symposium on Semiconductor Manufacturing Conference, Proceedings 1999, Pg. 65-68.

Nagesh, Sukhi et al., "Intelligent second-generation MES solutions for 300mm fabs", 2000, Solid State Technology, Vol. 43 No. 6, Pgs. 133-134, 136, 138.

These references are also listed on the accompanying Information Disclosure Statement (Form PTO-1449).

Consideration of the foregoing in relation to this patent application is respectfully requested.

Respectfully Submitted,



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(914)332-9081

Dated: November 7, 2005
Tarrytown, New York

U.S. Department of Commerce, Patent and Trademark Office

LIST OF RELEVANT ART CITED BY APPLICANT

(Use several sheets if necessary)

Docket No.:	Serial No.:
8201/Y01/SYNX/JW	10/764,620
Applicants: Michael R. Rice, et al	
Filing Date: January 26, 2004	Group: 2125

U.S. Patent Documents

*Examiner Initial		Document Number	Issue Date	Name	Class	Subclass	Filing Date If Appropriate
	US-1	5,544,350	08/06/96	Hung et al.			
	US-2	5,612,886	03/18/97	Yi-Cherng Weng			
	US-3	5,818,716	10/06/98	Chin et al.			
	US-4	5,825,650	10/20/98	Tza-Huei Wang			
	US-5	5,971,585	10/26/99	Dangat et al.			
	US-6	6,128,588	10/03/00	Guillermo Rudolfo Chacon			
	US-7	6,196,001	03/06/01	Tannous et al.			
	US-8	6,415,260	07/02/02	Yang et al.			
	US-9						
	US-10						
	US-11						

Foreign Patent Documents

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	F-1	JP 55091839 A	07/11/80	Japan			Abstract	
	F-2	JP 58028860 A	02/19/83	Japan			Abstract	
	F-3	JP 60049623 A	03/18/85	Japan			Abstract	
	F-4	JP 01181156 A	07/19/89	Japan			Abstract	
	F-5	JP 01257549 A	10/13/89	Japan			Abstract	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	OT-1	Przewlocki, H. et al., "DIASTEMOS-computerized system of IC manufacturing control and diagnostics", 1990, Elektronika, Vol. 31 No. 11-12, Pgs. 38-40, Polish Language. (Abstract only)
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	OT-3	Prasad, K., "A generic computer simulation model to characterize photolithography manufacturing area in an IC FAB facility", Sept. 1991, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 14 No. 3, Pg. 483-7.

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	US-12						
	US-13						
	US-14						
	US-15						
	US-16						
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	US-19						
	US-20						
	US-21						
	US-22						

Foreign Patent Documents

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	F-6	JP 02015647 A	01/19/90	Japan			Abstract	
	F-7	JP 05128131 A	05/25/93	Japan			Abstract	
	F-8	JP 05290053 A	11/05/93	Japan			Abstract	
	F-9	JP 06260545 A	09/16/94	Japan			Abstract	
	F-10	JP 08249044 A	09/27/96	Japan			Abstract	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	OT-4	Ehteshami, B. et al., "Trade-offs in cycle time management: hot lots", May 1992, IEEE Transactions on Semiconductor Manufacturing, Vol. 5 No. 2, Pg. 101-6.
	OT-5	Lou, S. et al., "Using simulation to test the robustness of various existing production control policies", 1991, 1991 Winter Simulation Conference Proceedings, IEEE, Pg. 261-9.
	OT-6	Berg, R. et al., " The formula: world class manufacturing for hybrid thin-film component production", 1992, IEEE/SEMI International Semiconductor Manufacturing Science Symposium, Pgs. 53-60.

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	US-33						

Foreign Patent Documents

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	F-11	JP 09115817 A	05/02/97	Japan			Abstract	
	F-12	JP 10135096 A	05/22/98	Japan			Abstract	
	F-13	JP 11176717 A	07/02/99	Japan			Abstract	
	F-14	JP 11296208 A	10/29/99	Japan			Abstract	
	F-15	JP 01332464 A	11/30/01	Japan			Abstract	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	OT-7	Naguib, H., "The implementation of total quality management in a semiconductor manufacturing operation", 1992, IEEE/SEMI International Semiconductor Manufacturing Science Symposium, Pg. 63-7.
	OT-8	Rose, D., " Productivity enhancement", 1992, IEEE/SEMI International Semiconductor Manufacturing Science Symposium, Pg. 68.
	OT-9	Narayanan, S. et al., "Object-oriented simulation to support operator decision making in semiconductor manufacturing", 1992, 1992 IEEE International Conference on Systems, Man and Cybernetics, Vol. 2, Pg 1510-15.

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	US-35						
	US-36						
	US-37						
	US-38						
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	US-41						
	US-42						
	US-43						
	US-44						

Foreign Patent Documents

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	F-16	JP 03007584 A	01/10/03	Japan			Abstract	
	F-17	DE 19715974 A1	10/22/98	Germany			Abstract	
	F-18	EP 1128246 A2	08/29/01	EPO			X	
	F-19							
	F-20							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	OT-10	Leonovich, G. A. et al., "Integrated cost and productivity learning in CMOS semiconductor manufacturing", Jan.-March 1995, IBM Journal of Research and Development, Vol. 39 No. 1-2, Pg. 201-13.
	OT-11	Leonovich, G., " An approach for optimizing WIP/cycle time/output in a semiconductor fabricator", 1994, Sixteenth IEEE/CPMT International Electronics Manufacturing Technology Symposium. 'Low-Cost Manufacturing Technologies for Tomorrow's Global Economy'. Proceedings 1994 IEMT Symposium, Vol. 1, Pg. 108-11.
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	US-54						
	US-55						

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	F-24							
	F-25							

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	OT-15	Houmin, Yan et al., "Testing the robustness of two-boundary control policies in semiconductor manufacturing", May 1996, IEEE Transactions on Semiconductor Manufacturing, Vol. 9 No. 2, Pg. 285-8.

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	US-56						
	US-57						
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	US-61						
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	US-64						
	US-65						
	US-66						

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	F-26							
	F-27							
	F-28							
	F-29							
	F-30							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	OT-16	Lopez, M. J. et al., "Performance models of systems of multiple cluster tools", 1996, Nineteenth IEEE/CPMT International Electronics Manufacturing Technology Symposium. Proceedings 1996 IEMT Symposium, Pgs. 57-65.
	OT-17	Collins, D. W. et al., "Implementation of Minimum Inventory Variability Scheduling 1-Step Ahead Policy(R) in a large semiconductor manufacturing facility", 1997, 1997 IEEE 6th International Conference on Emerging Technologies and Factory Automation Proceedings, Pgs. 497-504.
	OT-18	Labanowski, L., " Improving overall fabricator performance using the continuous improvement methodology", 1997, 1997 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop. Theme - The Quest for Semiconductor Manufacturing Excellence: Leading the Charge into the 21st Century. ASMC Proceedings, Pg. 405-9.

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	US-67						
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	US-69						
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	F-34							
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	US-88						

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	OT-22	Rose, O., " WIP evolution of a semiconductor factory after a bottleneck workcenter breakdown", 1998, 1998 Winter Simulation Conference. Proceedings, Vol. 2, Pgs. 997-1003.
	OT-23	Iriuchijima, K. et al., "WIP allocation planning for semiconductor factories", 1998, Proceedings of the 37th IEEE Conference on Decision and Control, Vol. 3, Pg. 2716-21.
	OT-24	Weiss, M., "New twists on 300 mm fab design and layout", July 1999, Semiconductor International, Vol. 22 No. 8, Pgs. 103-4, 106, 108.

Examiner	Date Considered.

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U.S. Department of Commerce, Patent and Trademark Office	Docket No.: 8201/Y01/SYNX/JW	Serial No.: 10/764,620
LIST OF RELEVANT ART CITED BY APPLICANT (Use several sheets if necessary)	Applicants: Michael R. Rice, et al	
	Filing Date: January 26, 2004	Group: 2125

U.S. Patent Documents

*Examiner Initial		Document Number	Issue Date	Name	Class	Subclass	Filing Date If Appropriate
	US-89						
	US-90						
	US-91						
	US-92						
	US-93						
	US-94						
	US-95						
	US-96						
	US-97						
	US-98						
	US-99						

Foreign Patent Documents

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	F-41							
	F-42							
	F-43							
	F-44							
	F-45							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	OT-25	Van Antwerp, K. et al., "Improving work-in-progress visibility with active product tags YASIC manufacture", Oct. 1999, Micro, Vol. 17 No. 9, Pgs. 67-9, 72-3.
	OT-26	Martin, D. P., " Total operational efficiency (TOE): the determination of two capacity and cycle time components and their relationship to productivity improvements in a semiconductor manufacturing line", 1999, 10th Annual IEEE/SEMI. Advanced Semiconductor Manufacturing Conference and Workshop. ASMC 99 Proceedings, Pgs. 37-41.
	OT-27	Martin, D. P., "Capacity and cycle time-throughput understanding system (CAC-TUS) an analysis tool to determine the components of capacity and cycle time in a semiconductor manufacturing line", 1999, 10th Annual IEEE/SEMI. Advanced Semiconductor Manufacturing Conference and Workshop. ASMC 99 Proceedings, Pg. 127-31.

Examiner	Date Considered

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U.S. Patent Documents

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	US-100						
	US-101						
	US-102						
	US-103						
	US-104						
	US-105						
	US-106						
	US-107						
	US-108						
	US-109						
	US-110						

Foreign Patent Documents

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	F-46							
	F-47							
	F-48							
	F-49							
	F-50							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	OT-28	Marcoux, P. et al., "Determining capacity loss from operational and technical deployment practices in a semiconductor manufacturing line", 1999, 1999 IEEE International Symposium on Semiconductor Manufacturing Conference Proceedings, Pg. 3-5.
	OT-29	Chen, J. C. et al., " Capacity planning for a twin fab", 1999, 1999 IEEE International Symposium on Semiconductor Manufacturing Conference Proceedings, Pg. 317-20.
	OT-30	Wei Jun-Hu et al., "Optimization methodology in simulation-based scheduling for semiconductor manufacturing", Oct. 2000, Information and Control, Vol. 29 No. 5, Pg. 425-30, Chinese language. (Abstract only)

Examiner	Date Considered

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U.S. Patent Documents

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	US-111						
	US-112						
	US-113						
	US-114						
	US-115						
	US-116						
	US-117						
	US-118						
	US-119						
	US-120						
	US-121						

Foreign Patent Documents

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	F-51							
	F-52							
	F-53							
	F-54							
	F-55							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	OT-31	Hughlett, E., " Incremental levels of automation in the compound semiconductor fab", Aug. 2001, Compound Semiconductor, Vol. 7 No. 7, Pg. 69-73.
	OT-32	Sarin, S. C. et al., "Reduction of average cycle time at a wafer fabrication facility", 2001, 2001 GaAs MANTECH Conference. Digest of Papers, Pg. 241-6.
	OT-33	Saito, K. et al., "A simulation study on periodical priority dispatching of WIP for product-mix fabrication", 2002, 13th Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference. Advancing the Science and Technology of Semiconductor Manufacturing. ASMC 2002, Pg. 33-7.

Examiner	Date Considered

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U.S. Patent Documents

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	US-122						
	US-123						
	US-124						
	US-125						
	US-126						
	US-127						
	US-128						
	US-129						
	US-130						
	US-131						
	US-132						

Foreign Patent Documents — Translation

		Document Number	Date	Country	Class	Subclass	Yes	No
	F-56							
	F-57							
	F-58							
	F-59							
	F-60							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	OT-34	Wang, J. et al., "The improvement of automated material handling system traffic control", 2002, 2002 Semiconductor Manufacturing Technology Workshop, Pg. 271-4.
	OT-35	Wei Jie Lee, "Optimize WIP scale through simulation approach with WIP, turn-over rate and cycle time regression analysis in semiconductor fabrication", 2002, 2002 Semiconductor Manufacturing Technology Workshop, Pg. 299-301.
	OT-36	Young Hoon Lee et al., "Push-pull production planning of the re-entrant process", 2003, International Journal of Advanced Manufacturing Technology, Vol. 22 No. 11-12, Pg. 922-31.

Examiner	Date Considered

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U.S. Patent Documents

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	US-133						
	US-134						
	US-135						
	US-136						
	US-137						
	US-138						
	US-139						
	US-140						
	US-141						
	US-142						
	US-143						

Foreign Patent Documents — Translation

		Document Number	Date	Country	Class	Subclass	Yes	No
	F-61							
	F-62							
	F-63							
	F-64							
	F-65							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	OT-37	Garlid, Scott C., "From philosophy to reality. Interpreting the rules of JIT for IC manufacturing", 1989, SME Technical Paper (Series) MS. Publ by SME, Pg. 797.
	OT-38	Anon, " Wafer level automation", Jan. 1995, European Semiconductor, Vol. 17 No. 1, Pg. 2.
	OT-39	Anon, "Coming of fab-wide automation", May 1998, European Semiconductor Design Production Assembly, Vol. 20 No. 5, Pg. 21-22.

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	US-144						
	US-145						
	US-146						
	US-147						
	US-148						
	US-149						
	US-150						
	US-151						
	US-152						
	US-153						
	US-154						

Foreign Patent Documents — Translation

		Document Number	Date	Country	Class	Subclass	Yes	No
	F-66							
	F-67							
	F-68							
	F-69							
	F-70							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	OT-40	Pierce, Neal G. et al., " Dynamic dispatch and graphical monitoring system", 1999, IEEE International Symposium on Semiconductor Manufacturing Conference, Proceedings 1999, Pg. 65-68.
	OT-41	Nagesh, Sukhi et al., " Intelligent second-generation MES solutions for 300mm fabs", 2000, Solid State Technology, Vol. 43 No. 6, Pgs. 133-134, 136, 138.
	OT-42	

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